# Abstract: Add an RS-232 Port to an EPLD By Steven W. Cole Jet Propulsion Laboratory, California Institute of Technology

### Why add an RS-232 Port to a Small System

As EPLDs become part of small systems the level of integration is increased, cost and time to market go down. Unfortunately, EPLDs hide hardware where a logic analyzer can not be effective. Also, as EPLDs become larger, the amount of free space within the EPLD not used by the basic design becomes larger. An RS-232 UART can be placed in this free space to add a window into the system.

### **Principle of Operation**

The basic method employed in the implementations discussed here uses a clock at 3 times the BAUD rate. When the start bit is detected twice on adjacent clock cycles, the method starts shifting the character bits in with every third clock edge thereafter. This places the input sampling shift clock in the center 1/3 of each bit. The method can inherently tolerate a 3% total BAUD rate error. Transmission is easier. Here, every third edge of the 3-times-BAUD-clock is used to shift data out. When the transmitter is idle, an output sequence can begin on any 3-times-BAUD-clock edge. A hardware intensive implementation is discussed.

## The Implementation Took

The following implementations were done using MAX+PLUS II, the EPLD development system sold by Alters Corp. The elements of the development system I used include a schematic editor, compiler, simulator, and waveform editor.

# 'I'he Implementation

This implementation requires 48 flip-flops. The implementation provides the highest possible BAUD rate and the lowest required interaction by the processor. This implementation is fully synchronous. The receiver and transmitter each contain a 3 or 4 bit **shift** counter, 8 bit **shift** register, 8 bit holding register, parity generator/checker, interrupt flag flip-flop, and a 3 bit state machine.

### Conclusion

I have found that almost every system is helped by the addition of an RS-232 port. Think of what it could do for your project. Providing the structure of a UART in an EPLD allows the designer to customize it to implement the standard in the way best suited to his or her project. The implementation discussed here is provided as a starting point, not as a cook-book.